

CBCS SCHEME

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18EC34

Third Semester B.E. Degree Examination, Jan./Feb. 2021 Digital System Design

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

- 1 a. Design a logic circuit that has 4 inputs, the output will be high, when the majority of the inputs are high. Use K-map to simplify. (07 Marks)
- b. Express the following functions into canonical form:
(i) $f_1 = ab' + ab' + bc$ (ii) $f_2 = (a + b')(b' + c)$ (06 Marks)
- c. Identify all the prime implicants and essential prime implicants of the following using K-map.
i) $f(a, b, c, d) = \Sigma m(6, 7, 9, 10, 13) + dc(1, 4, 5, 11, 15)$
ii) $f(a, b, c, d) = \pi M(1, 2, 3, 4, 9, 10) + dc(0, 14, 15)$
iii) $F(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$ (07 Marks)

OR

- 2 a. Simplify the following using tabulation methods:
 $Y = \Sigma m(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d(4, 8, 11)$ (07 Marks)
- b. Simplify the following expression using K-map. Implement the simplified expression using NAND gates only. $F = \Sigma m(0, 1, 2, 5, 6, 7, 8, 9, 10, 13, 14, 15)$. (07 Marks)
- c. Explain briefly K-map, incompletely specified functions, essential prime implicants and gray codes. (06 Marks)

Module-2

- 3 a. Design a two bit magnitude comparator. (10 Marks)
- b. Realize the following functions expressed in maxterm canonical form in two possible ways using 3:8 decodes. $f_1(a, b, c) = \pi M(1, 2, 6, 7)$ and $f_2(a, b, c) = \pi M(1, 3, 6, 7)$ (10 Marks)

OR

- 4 a. Implement $f(a, b, c, d) = \Sigma m(0, 1, 5, 6, 7, 9, 10, 15)$, using;
(i) 8:1 mux with a, b, c, as select lines (ii) 4:1 mux with a, b as select lines. (08 Marks)
- b. Explain 4-bit carry look-ahead adder with necessary diagram and relevant expressions. (04 Marks)
- c. Draw a PLA circuit to implement the logic function $A'BC + AB'C + AC'$ and $A'B'C' + BC$. (08 Marks)

Module-3

- 5 a. Explain with timing diagrams the workings of SR latch as a switch debouncer. (08 Marks)
- b. What is race around condition? Explain JK Master Slave flipflop with a diagram, function table and timing diagram. (07 Marks)
- c. List the difference between combinational and sequential circuits. (05 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 6 a. Explain the operation of clocked SR flipflop using NAND gates. (07 Marks)
b. What is the significance of Edge Triggering? Explain the working of positive edge triggered D-FF with their function table. (07 Marks)
c. Explain the working of 4-bit twisted ring counter using necessary diagram and logic table. (06 Marks)

Module-4

- 7 a. Using positive edge triggering SR flipflops design a counter which counts in the following sequence: 000, 111, 110, 101, 100, 011, 010, 001, 000 ... (10 Marks)
b. Design a synchronous mod-6 counter using D-flipflop to generate the sequence (0, 2, 3, 6, 5, 1, 0) (10 Marks)

OR

- 8 a. Write the difference between Mealy and Moore model with necessary diagrams. (10 Marks)
b. Explain state machine notations with an example. (10 Marks)

Module-5

- 9 a. Construct Mealy state diagram that will detect input sequence 10110, when input pattern is detected, Z is asserted high. Give state diagram for each state. (10 Marks)
b. With necessary diagram, explain the concept of serial adder with accumulators. (10 Marks)

OR

- 10 a. Design a sequential circuit to convert BCD to excess 3 code. (10 Marks)
b. Explain the design of sequential circuit using CPLD's and give CPLD implementation of a shift register and parallel adder with accumulator. (10 Marks)
